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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRAN, TAN N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,134	SHIMIZUME, KAZUTOSHI	
	Examiner	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on05/05/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The indicated allowability of claims 2,3,5 is withdrawn in view of the newly discovered reference(s) to claims 2,3,5. Rejections based on the newly cited reference(s) follow.

Information Disclosure Statement

2. If applicant is aware of any relevant prior art, he/she requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. **609.**

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (6,446,249) in view of Gilliam (5,566,107).

With regard to claims 1,2, Wang et al. discloses an I/O region formed on a chip 425 and having at least an input/output pad 435; a plurality of active region 505 formed on the chip 425; the active region 505 being separated from one another by a boundary spacer; a plurality of logic circuits having either one of the same functions and different functions being mounted in each of the active regions 505, and a selection circuit (Note fig. 14) for selectively operating only one of the plurality of mounted logic circuits. (Note figs. 1B, 10,11,14 of Wang et al.).

Wang et al. does not disclose each of plurality of mounted logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level, and selection circuit includes a disconnecting section, the disconnecting section is disconnected to allow permanent setting of an operable circuit.

However, Gilliam discloses a selection circuit 26 for selectively operating only one of the plurality of mounted logic circuit 18; each of the plurality of mounted logic circuit 18 is operated by setting an SEL signal for turning on/off a transistor 82(84) for each of the mounted logic circuit 18 to one of a high and a low level, and selection circuit 26 includes a disconnecting section 62, the disconnecting section 62 is disconnected to allow permanent setting of an operable circuit. (Note figs. 1,3 of Gilliam).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level and selection circuit includes a disconnecting section, the disconnecting section is disconnected to allow permanent setting of an operable circuit such as taught by Gilliam for enabling an associated function circuit in response to an activate signal.

With regard to claim 3, Gilliam discloses the disconnecting section 62 includes a fuse. (Note figs. 1,3 of Gilliam).

With regard to claims 4,5, Wang et al. discloses an I/O region formed on a chip 425 and having at least an input/output pad 435; a plurality of active region 505 formed on the chip 425; the active region 505 being separated from one another by a boundary spacer; a plurality of logic circuits having either one of the same functions and different functions being mounted in each of

the active regions 505, and a selection circuit (Note fig. 14) for selectively operating only one of the plurality of mounted logic circuits. (Note figs. 1B, 10,11,14 of Wang et al.).

Wang et al. does not disclose the selection circuit includes a transistor element connected in series with each the logic circuit between the logic circuit and a power terminal; the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through the input/output pad.

However, Gilliam discloses the selection circuit 26 includes a transistor element 60 connected in series with the logic circuit 72 between the logic circuit 72 and a power terminal Vcc, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through activate signal serves as the input/output pad. (Note fig. 3 of Gilliam).

Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the selection circuit includes a transistor element connected in series with each the logic circuit between the logic circuit and a power terminal, the selection circuit or transistor element selects a logic circuit to be operated on a basis of a signal input supplied from an outside through activate signal serves as the input/output pad such as taught by Gilliam in order to enabling an associated function circuit in response to an activate signal.

Response to Arguments

4. Applicant's arguments filed 05/05/03 have been fully considered but they are not persuasive.

It is argued, at page 4 of the remarks, that "Wang et al. do not teach or suggest a semiconductor device including a selection circuit for selectively operating only one of the plurality of mounted logic circuits, wherein each of the plurality of mounted logic circuits is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuits, to one of a high and a low level". However, figs. 1,3 of Gilliam does show a selection circuit 26 for selectively operating only one of the plurality of mounted logic circuit 18; each of the plurality of mounted logic circuit 18 is operated by setting an SEL signal for turning on/off a transistor 82(84) for each of the mounted logic circuit 18 to one of a high and a low level. Therefore, it would have been obvious to one of ordinary skill in the art to form the Wang et al.'s device having the logic circuit is operated by setting an SEL signal for turning on/off a transistor for each of the mounted logic circuit to one of a high and a low level such as taught by Gilliam in order to enabling an associated function circuit in response to an activate signal. Thus, Applicant's claims 1-5 do not distinguish over Gilliam and Wang et al. references.

Conclusion

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

July 2003

Minhloan Tran
Primary Examiner
Art Unit 2826